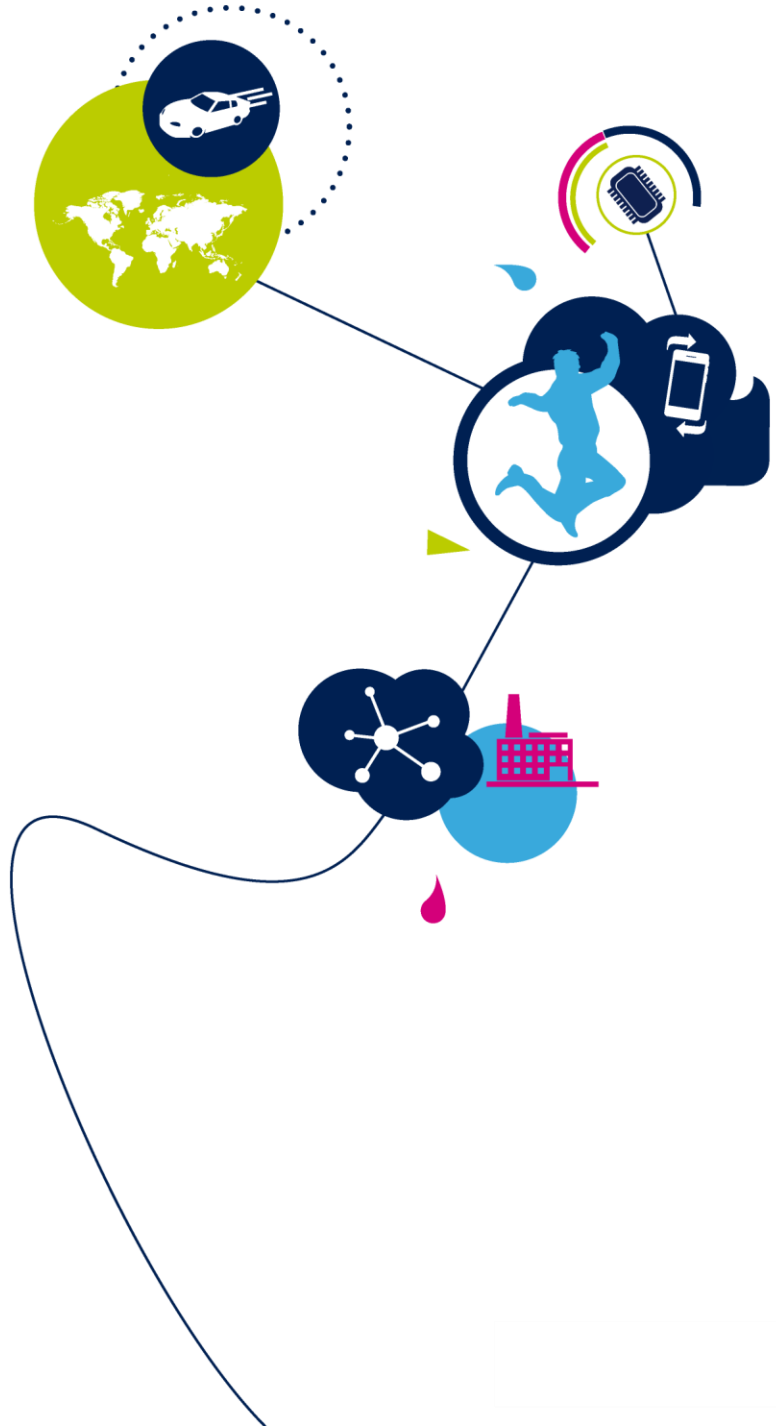
STM32H7- ARM® 内核



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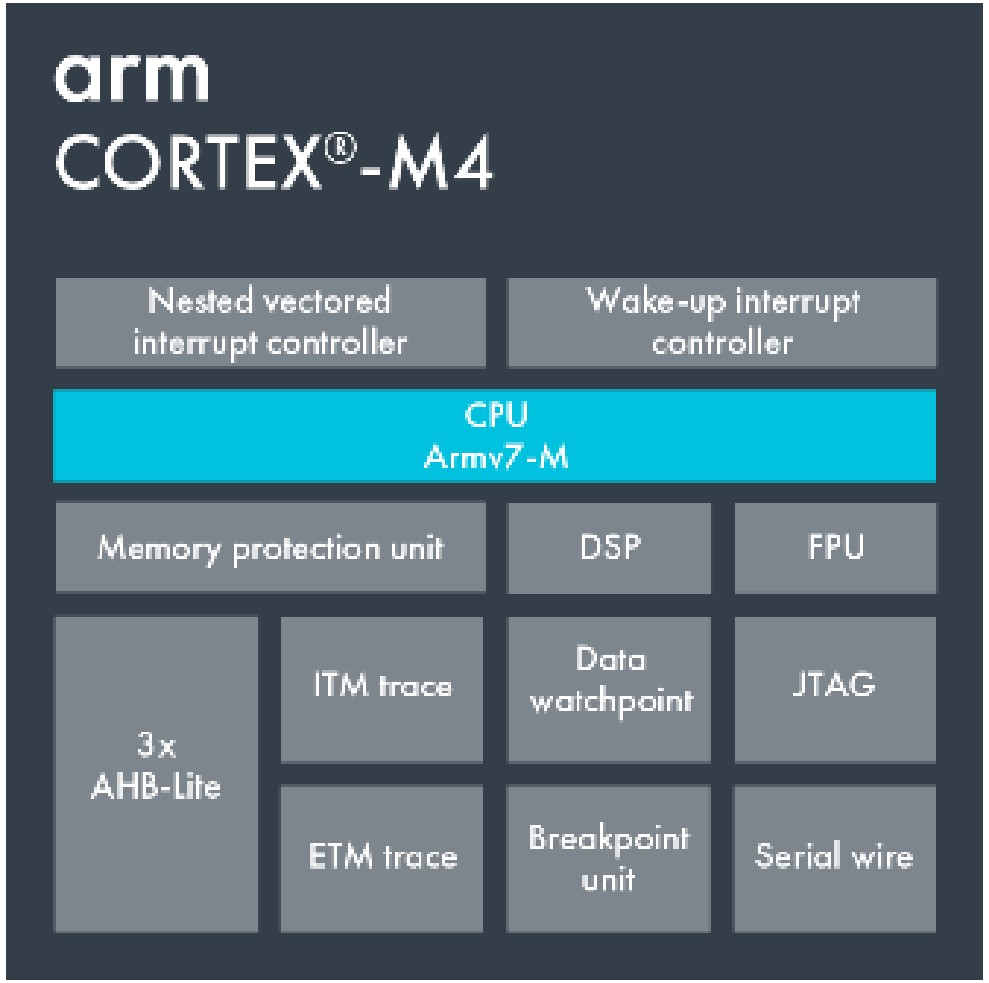
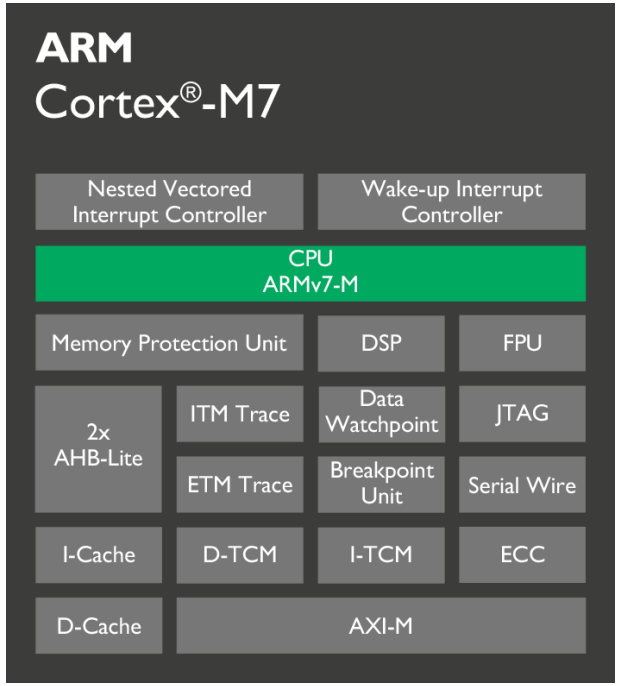
Cortex-M4 处理器概述



Cortex-M7 处理器概述

- ARMv7E-M 架构
- Harvard 结构, 6-stage 流水线
- 超标量双发射架构!
- DIV 最大需要 12 周期 (max.), SIMD 指令
- 内存保护单元Memory Protection Unit (MPU)
- 单 和 双 精度 Floating Point Unit (FPU)

  ⇒ 包含STM32H7使用的 ARM Cortex®-M7



更接近DSPs	更接近Real-Time 处理器
Load and store in parallel with arithmetic operations	Tightly Coupled Memories(TCM)
Zero overhead loops	AXI-M interface with Cache memory

Cortex-M 兼容性

- 忘记传统的 8/16/32位MCU划分
  - 所有应用都可以使用的无缝的架构
  - 每个产品都具有低功耗和易用的特性

Cortex-M0 & M0+	Cortex-M3	Cortex-M4	Cortex-M7
8/16-bit applications	16/32-bit” applications	32-bit/DSC applications	

二进制代码和工具兼容

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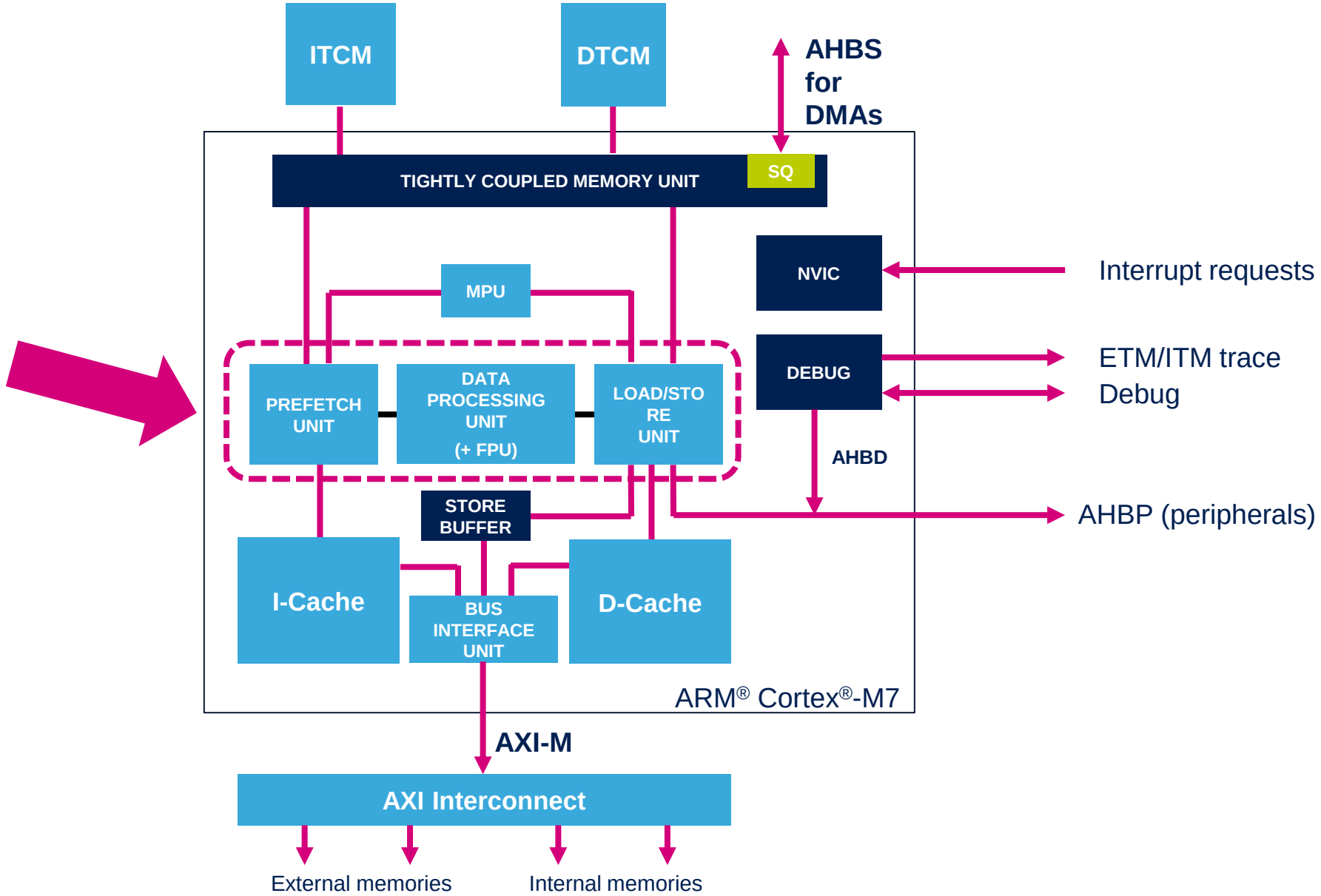
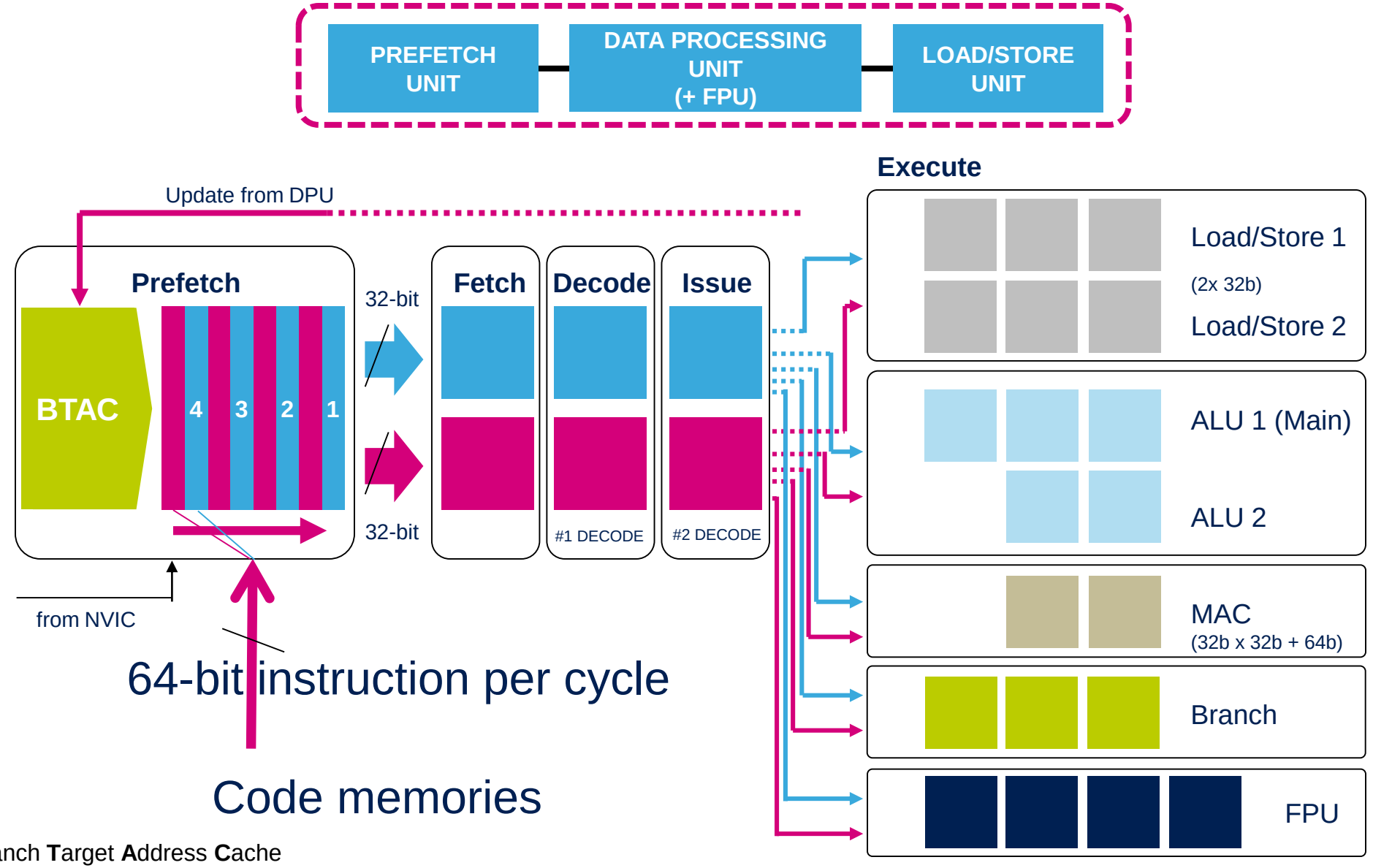
内核架构总览



ARM Cortex-M7 → 双发射

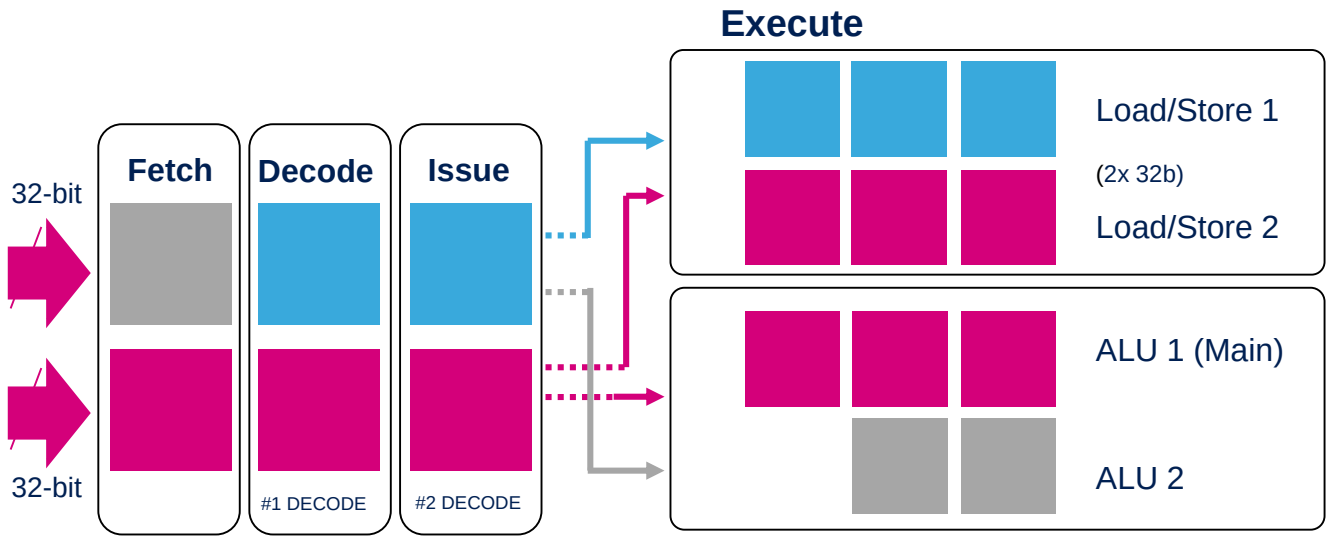


Branch **T**arget **A**ddress **C**ache

Load 和 store 并行的操作

- Cortex®-M7 内核
  - 没有延时的内存访问

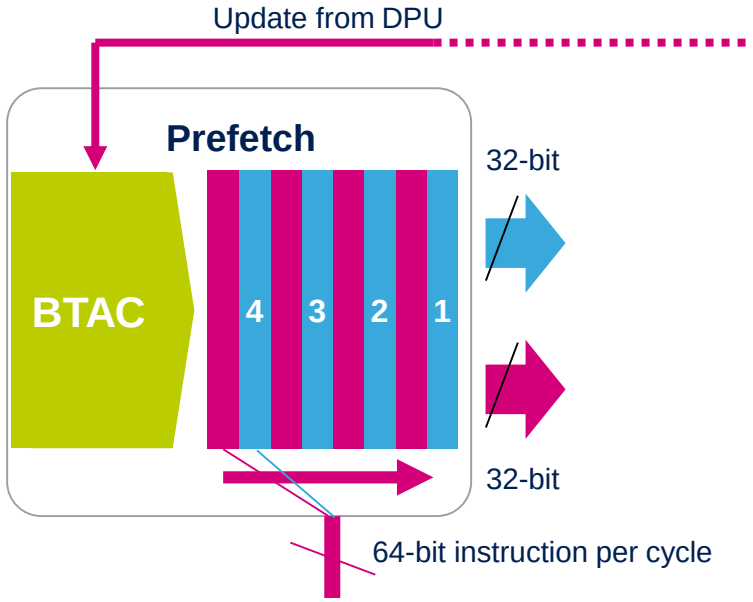
Interleave memory accesses with computation



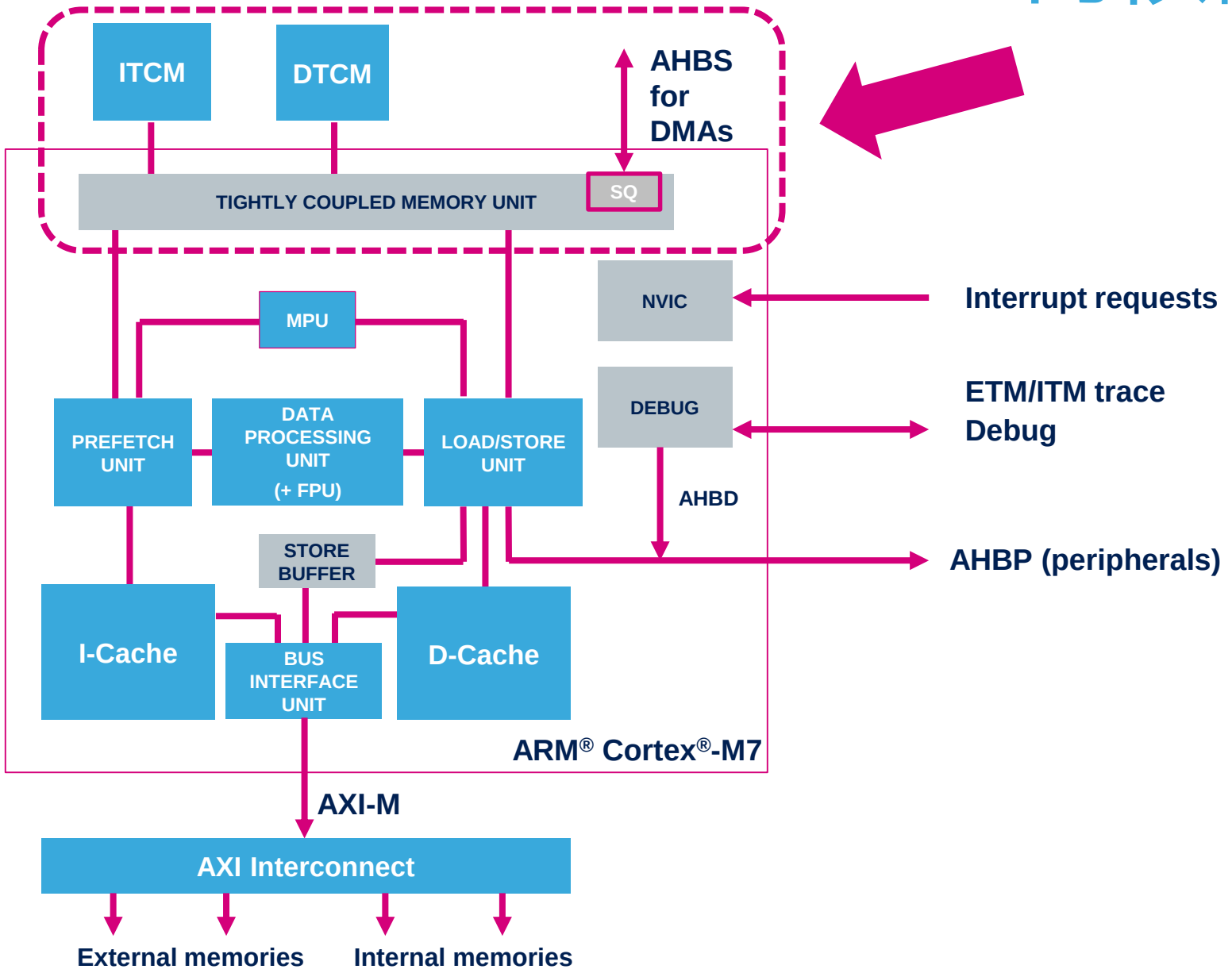
Compiler job!

零开销循环Zero overhead loops

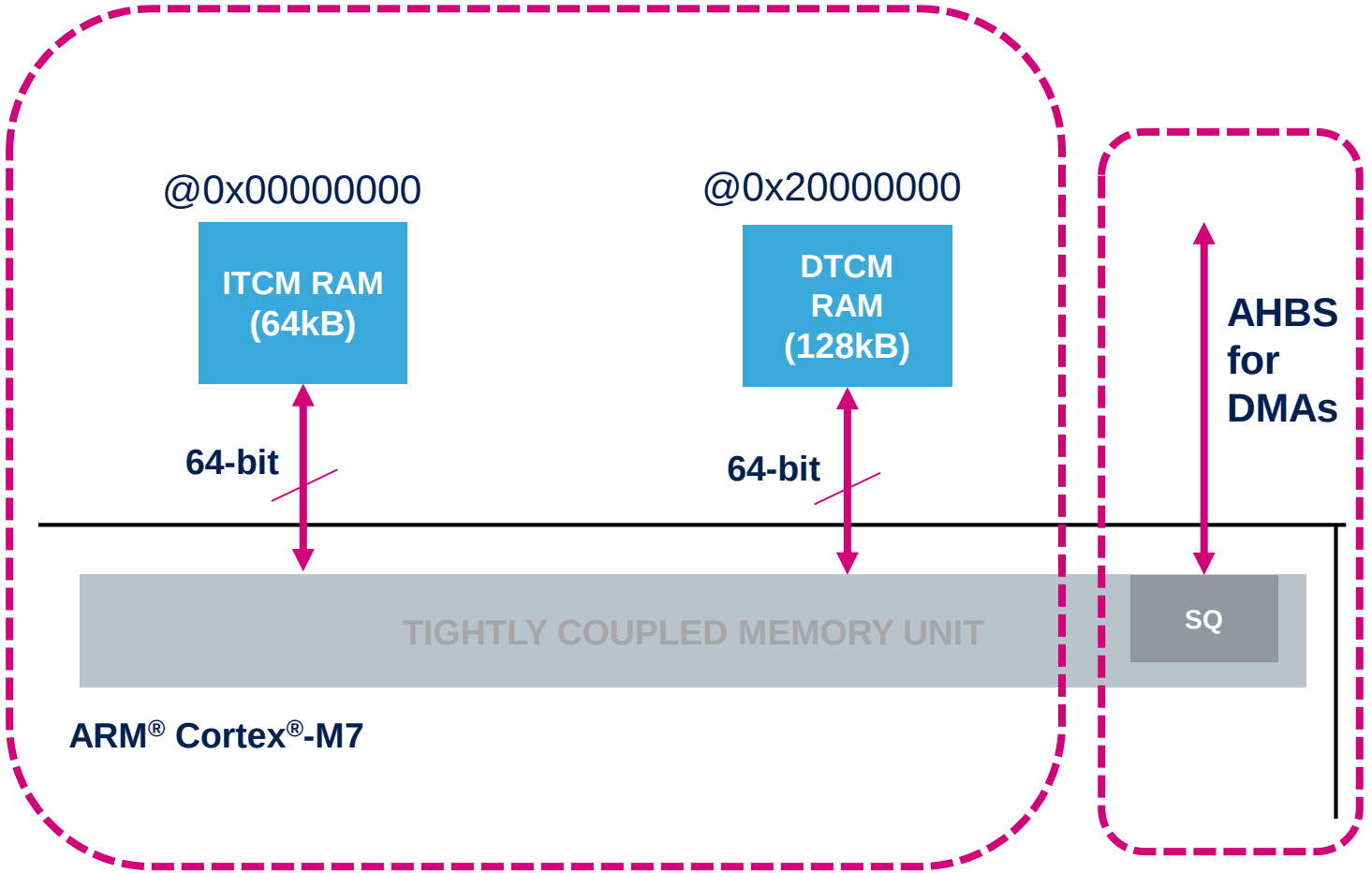
- 带条件的循环需要增加 / 减少 + 分支执行
- 在 Cortex-M7: 可以用分支预取和超标量双发射的结构，实现一个周期的条件循环执行



内核概览



Tightly coupled memories (TCM)



紧密耦合存储器 不需要等待周期0 wait states

Tightly coupled memories (TCM)

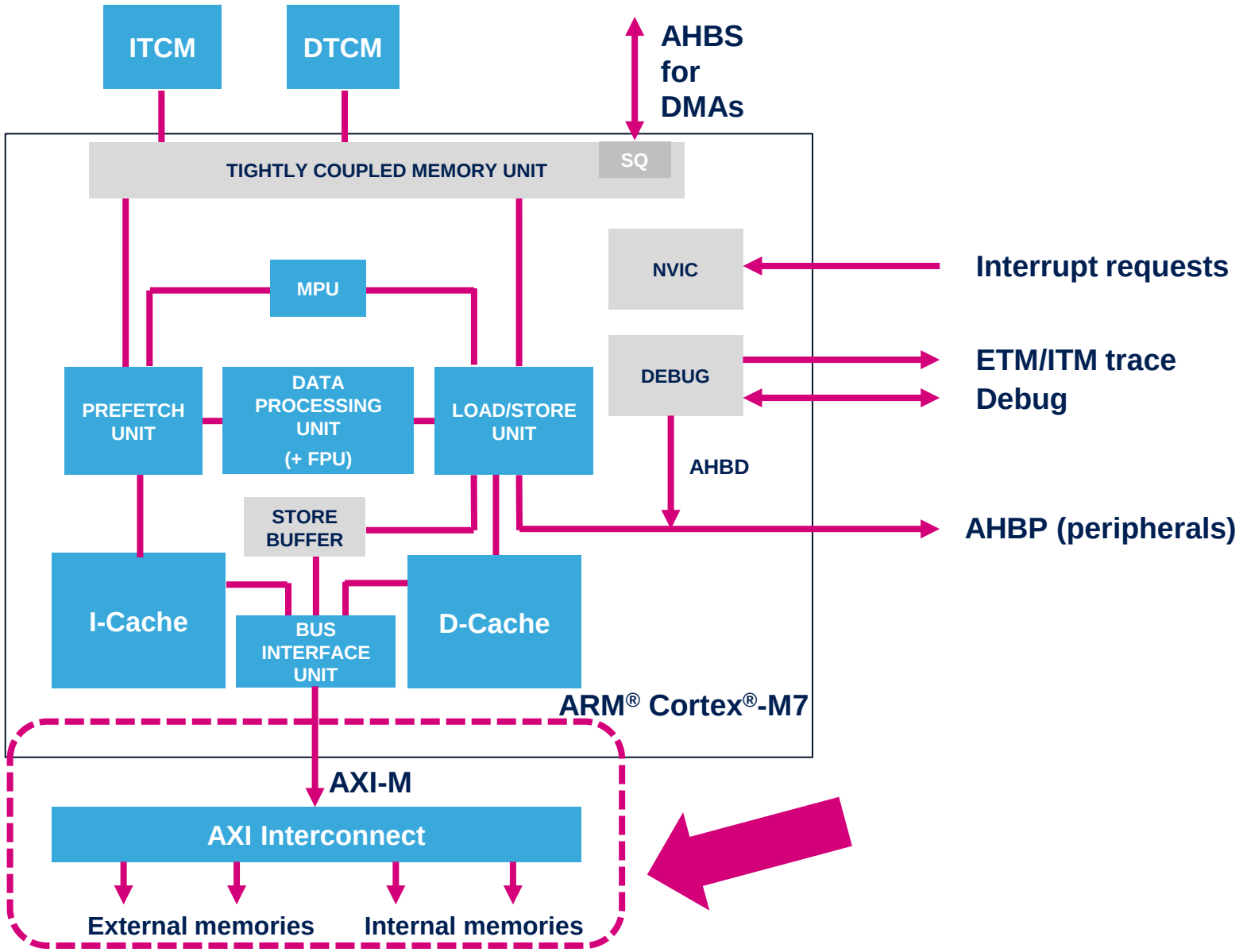
ITCM RAM (64 Kbytes)

- 关键代码
- 中断服务程序
- 高确定性延时要求

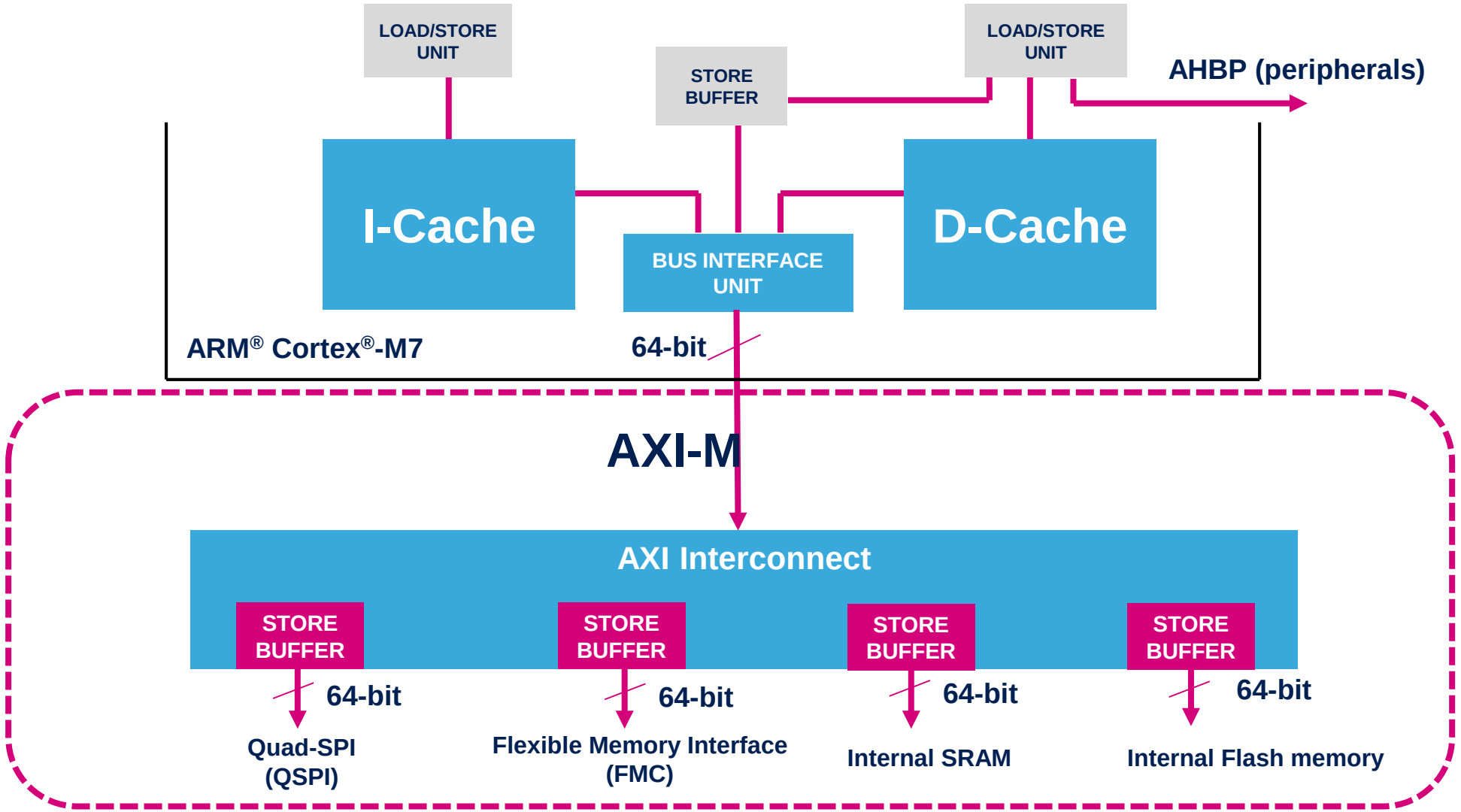
DTCM RAM (128 Kbytes)

- 频繁使用的数据
- Stack/Heap
- DSP 系数

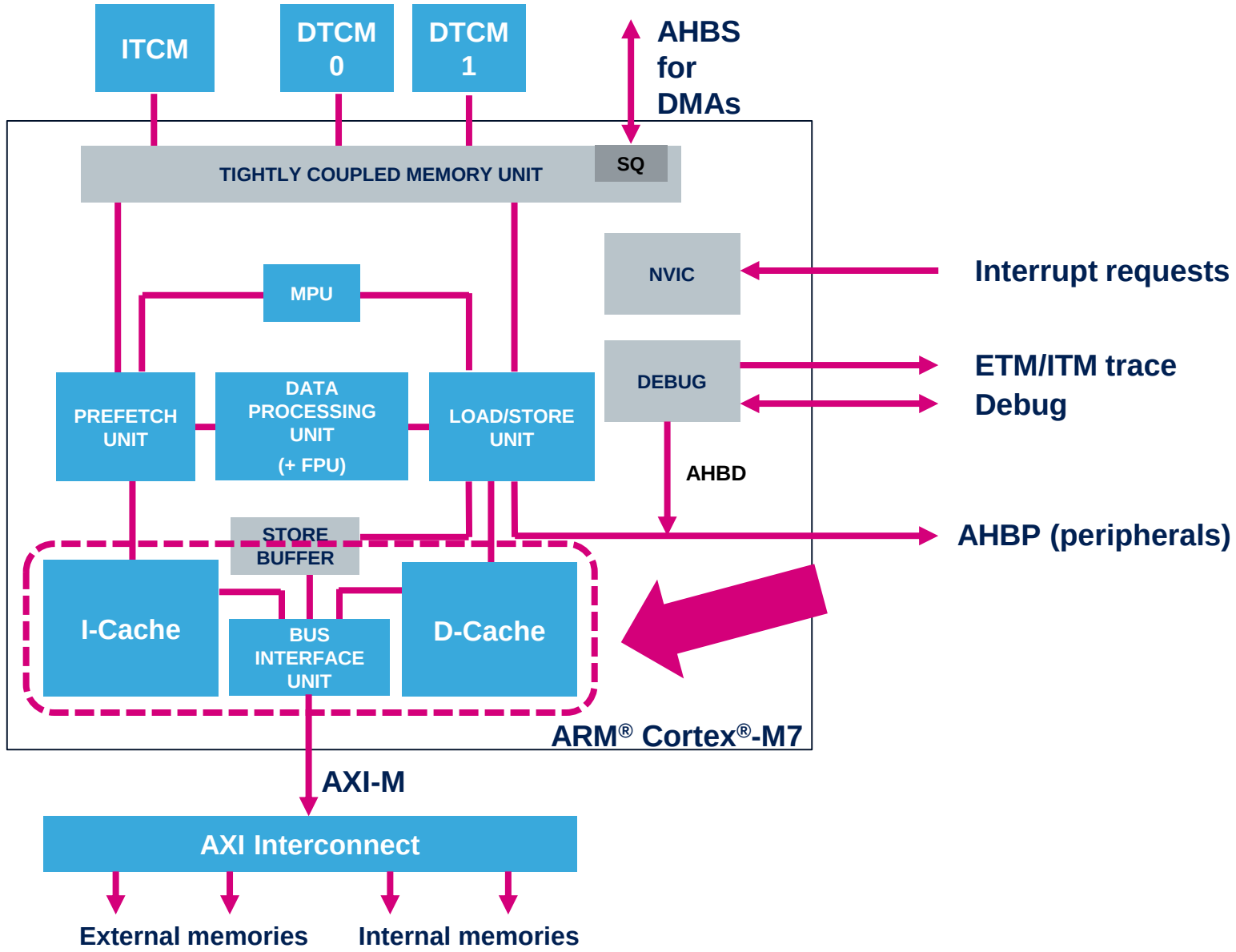
内核结构概述



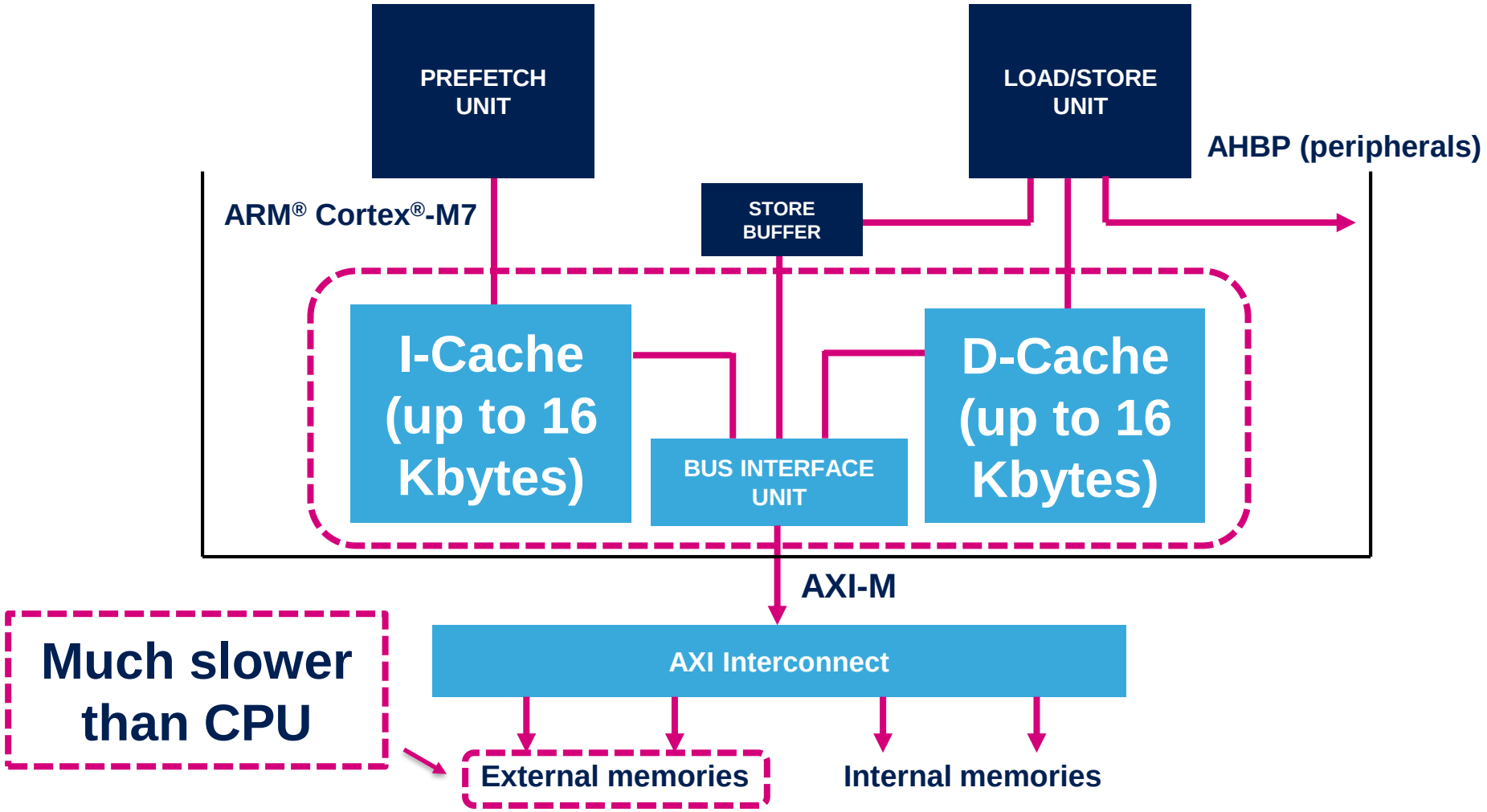
AXI-M 接口



内核概览



AXI-M 上的 L1 cache

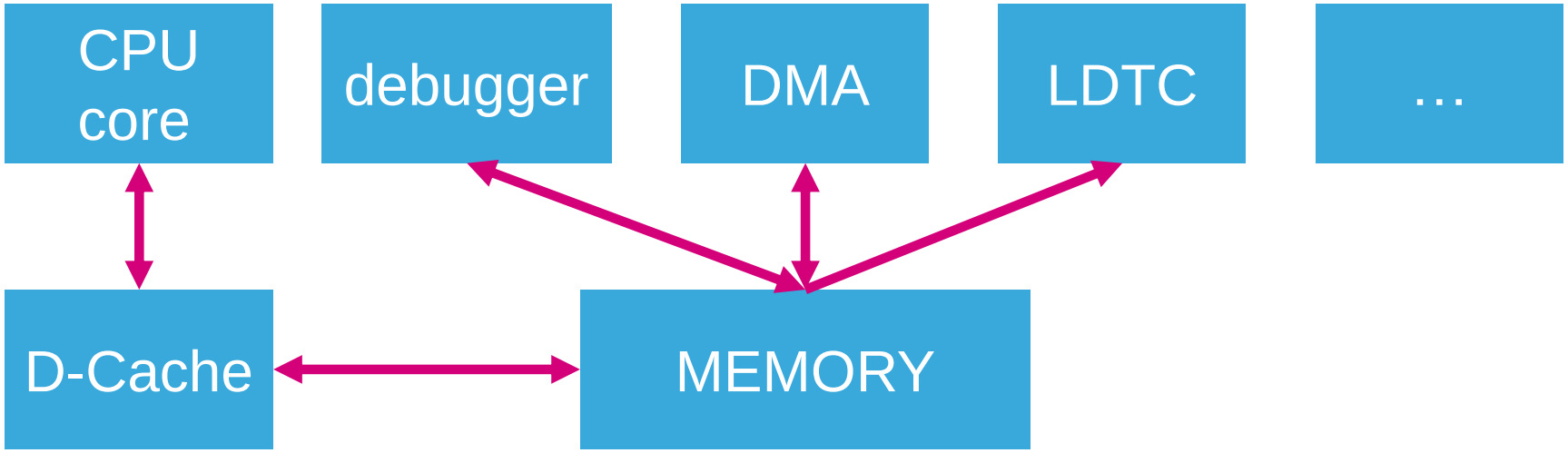


Cache RAM ECC

内置的 Error Checking and Correction

- Cortex-M7 cache, 内核来控制 ECC
  - 启动后默认ECC是使能的
  - Cache ECC 可以通过修改CM7_CACR.ECCEN来改变
  - CM7_CACR （cache configuration） 只有在下列情况下才可以被改动:
    - 两个cache都被关断
    - 整个cache 必须被invalidated （需要做flush操作），当ECC保护被改动后
- ECC 机制基于SECDED 算法.

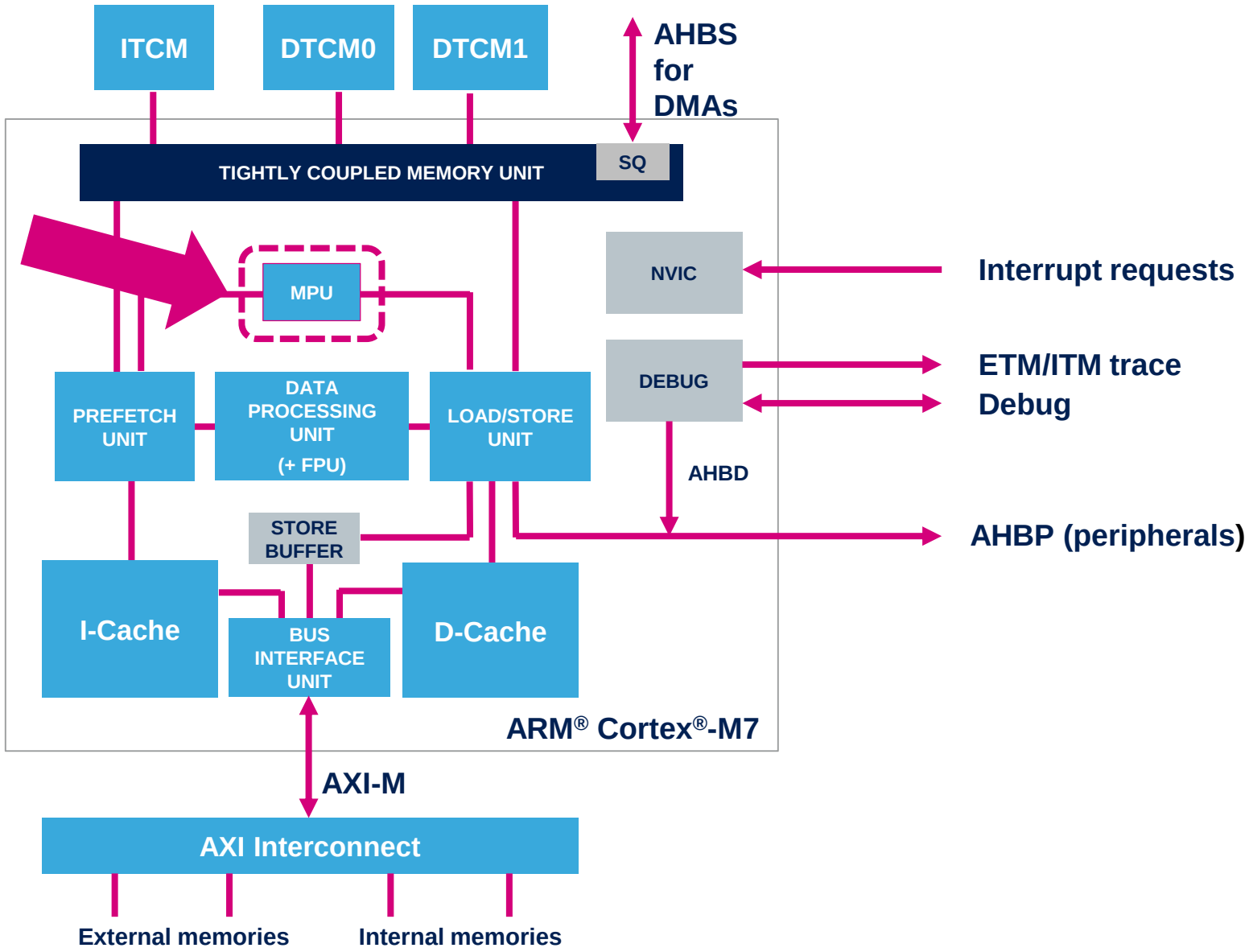
Data cache 一致性问题



如何解决cache一直性问题:

1. Don’t use cache at all (mark region as shared or not-cacheable)
2. Invalidate cache when you pass control to another master
3. In case of write only, you can use Write-Through policy

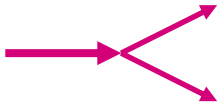
内核概览



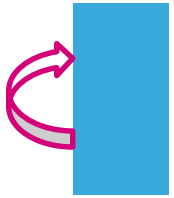
Memory protection unit and cache

- MPU 属性设置用来控制 AXI-M/Cache 的行为
- 可以把整个存储空间划分为16 个相互独立的，有不同属性的存储区
  - Cache On / Off
  - Cache Policy
  - Can execute code
  - Unprivileged mode access

STM32H7内核总结

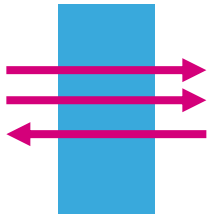


1. Superscalar → 2 instructions in 1 cycle



2. Branch in 1 cycle

3. Cache system to compensate slow memories



4. High system bandwidth for every application

参考

- For more details, please refer to the following documentation:
  - STM32F7 Series and STM32H7 Series Cortex®-M7 processor programming manual (PM0253)
  - Managing memory protection unit (MPU) in STM32 MCUs (AN4838)
  - Level 1 cache on STM32F7 series (AN4839)
  - STM32H7x3 system architecture and performance (AN4891)
  - ARM website at the following link:
    - http://www.arm.com/products/processors/cortex-m/cortex-m7-processor.php